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DESIGN, PROCESSING, AND TESTING OF LSI ARRAYS FOR SPACE STATION

BY

W. C. SCHNEIDER

QUARTERLY TECHNICAL REPORT NO. 15

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15. Supplementary Notes

16. Abstract

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SUMMARY

A significant milestone was reached this quarter when, at wafer probe, units of the TA6567 circuit, a beam-leaded COS/MOS/SOS 256-bit RAM, were demonstrated to be functionally perfect. Under previous support for this research program, an aluminum-gate current-sense version and a silicon-gate voltage-sense version of this memory were developed. Initial base line data for the beam-lead SOS process using the TA5388 circuit show the stability of the dc device characteristics through the beam-lead processing.

I. INTRODUCTION

RCA research and development of SOS technology covers many facets, including materials and basic device research, computer-aided design, mask-making techniques, and advanced CMOS array design using large-scale integration (LSI). This research and development program has been partially supported under the present NASA contract to develop a beam-lead technology that is compatible with the standard CMOS/SOS silicon-gate technology. The vehicle chosen to demonstrate achievement of the above goal was the 256-word by 1-bit RAM circuit.

The evolution of this research program saw the development of an aluminum-gate current-sense version followed by a silicon-gate voltage-sense version of this memory. The latter version of the memory has performed almost exactly as predicted in the computer-aided design simulation. In parallel with the memory work was the development of the beam-lead SOS technology, using the TA5388 dual-complementary pair plus inverter circuit as a test vehicle. This new technology has combined the standard SOS technology with a modified microbridge beam-lead (BL) technology. All phases of this technology were investigated, including development of a process for laser-scribing, separating, and bonding the BL/SOS chips to a DIP ceramic substrate. Mechanical samples of both BL/SOS TA5388 and TA6567 circuits were delivered to NASA, Huntsville, Alabama.

During this quarter, wafer testing of the BL/SOS TA6567 circuit has demonstrated that the units are functionally perfect; i.e., units have been found which successfully pass MARCH, MASEST, GALPAT, and WAKPAT test routines on the MD-100 memory exerciser. Packaged units have not been available for further testing. The initial device dc electrical base line data for the BL/SOS process using the TA5388 circuit are being established.

II. ELECTRICAL RESULTS ON BEAM-LEADED SOS TA5388 DEVICES

In this phase of the contract the electrical base line data for the beam-leaded SOS process are being established. The data reported in this section are a part of the overall characterization of this process and should be used only in the context in which they are presented.

The electrical data are part of an experiment to determine the effect on the device dc characteristics of varying the thickness of the Si_3N_4 passivation layer. The results are for Si_3N_4 layers 500 Å, 1200 Å, and 2000 Å thick on the BL/SOS TA5388 circuits at the wafer probe using the Integrated Circuit Tester (ICT). The values listed in Table 1 and in Table 2 are average values of measurements made on individual devices over a 1.5-in.-diameter wafer. The total number of measurements for each average value was between 100 and 265, depending on the time available on the ICT when that wafer was tested.

Table 1 summarizes the yield data for the standard silicon-gate deep-depletion SOS process for the three different thicknesses of the Si_3N_4 passivation layer as measured on the control wafer with aluminum metallization (control Al metal) and on the beam-leaded wafer after Ti/Pd/Au base metallization (Au I) and again after formation of the gold beams (Au II). These wafers were processed as one lot through the contact-opening step in the process, except for the deposition of the Si_3N_4 passivation layer. The wafers for any given Si_3N_4 thickness were processed exactly the same up to metallization, and they provide the most meaningful data for comparison. The data for Au I and Au II on wafers SW27-1, SW28-1, and SW28-3 for a given Si_3N_4 thickness were measured on the same wafer after the base metal processing and after the beam formation, respectively. In general, the beam-lead wafers had higher yield than the aluminum control wafers, and the wafers with the 500-Å-thick Si_3N_4 layer had the highest yield. A word of caution on the use and interpretation of these yield figures is in order. The yield is a strong function of the size and type of circuit and the type of tests

used to define the yield. These figures should not be considered yield figures for the standard SOS process but only as a relative comparison in this experiment.

Table 1. TA5388 Wafer Yield

Si_3N_4 Thickness	500 Å		1200 Å		2000 Å	
	Wafer #	% Yield	Wafer #	% Yield	Wafer #	% Yield
Control Al Metal	SW27-3	26.2	SW28-2	14.6	SW28-5	10.0*
Au I	SW27-1	64.2	SW27-4	10.4	SW28-4	39.7
	SW27-2	65	SW28-1	22.8	SW28-3	10.6
			SW27-5	23.4		
Au II	SW27-1	67.9	SW28-1	23.8	SW28-3	11.9

*The % yield for these conditions was actually measured as 18%, using a higher I_L value specification in the test program. The 10% value is an estimate based on the distribution of values in the "statistical print-out" to match the level of I_L values used to calculate the other yield values in the table.

The average values at wafer probe for dc device parameters at V_{DD} = 10 volts are given in Table 2. The parameters are leakage current (I_L) measured in nA/mil, threshold voltage (V_T) at 10 µA, transconductance (g_m) in µmhos, and source-to-drain breakdown voltage (V_{BD}) in volts, measured at 50 µA. The subscripts P and N are for the PMOS and NMOS transistors, respectively. The alphanumeric designation for the wafer is given in parentheses on the left of the I_{LP} values. The values for the other device parameters are listed in the same order as for I_{LP}.

A meaningful parameter for this discussion is V_T, since it is a sensitive indication of the effect of processing on the electrical device characteristics. The other parameters in Table 2 are included to show the stability of the device parameters through the beam-lead

Table 2. TA5388 Average DC Device Parameters, V_{DD} = 10 Volts

	Si_3N_4 Thickness (Å)	Al Metal Control		Au I		Au II	
I_{LP} (nA/mil)	500	(SW27-3)	1.0	(SW27-1)	0.8	(SW27-1)	0.9
	1200	(SW28-2)	0.4	(SW28-1)	0.5	(SW28-1)	0.6
	2000	(SW28-5)	3.5	(SW28-3)	0.7	(SW28-3)	1.0
I_{LN} (nA/mil)	500		-2.6		-0.7		-0.6
	1200		-2.5		-3.2		-3.1
	2000		-5.3		-3.9		-2.9
V_{TP} (volts) @ 50 µA	500		-0.68		-0.86		-0.84
	1200		-1.03		-0.82		-0.82
	2000		-0.89		-0.87		-0.87
V_{TN} (volts)	500		1.17		1.53		1.55
	1200		1.37		1.45		1.42
	2000		1.26		1.41		1.19
g_{mP} (µmhos)	500		1520		1164		1177
	1200		1090		1200		1210
	2000		1170		1240		1245
g_{mN} (µmhos)	500		995		768		760
	1200		800		825		825
	2000		850		950		910
$V_{BD(P)}$ (volts) @ 50 µA	500		-26.2		-29.0		-28.9
	1200		-27.9		-26.9		-26.8
	2000		-27.0		-28.1		-27.5
$V_{BD(N)}$ (volts)	500		21.1		25.8		25.8
	1200		26.6		25.0		25.1
	2000		25.3		26.2		26.5

processing. The values for Au I and Au II remained basically the same, indicating that the gold beam formation process does not drastically change the device characteristics. The values of V_{TP} for Au I and Au II and for all Si_3N_4 thicknesses are consistent within 0.05 volt. The values of V_{TN} for Au I and Au II also show this consistency for 500-Å and 1200-Å Si_3N_4 thicknesses. A slightly larger variation for V_{TN} at 2000 Å is related to the change in I_{LN} at that thickness of Si_3N_4. In most cases the aluminum metal control V_{TH} values differ from the beam-lead device values, but the distribution of values for each parameter is basically the same.

The distribution of the threshold voltages for the cases listed in Table 2 are shown in the histograms (Figs. 1 through 18).*

The V_{TP} histograms are shown in Figs. 1 through 9; they are grouped according to Si_3N_4 thickness (500 Å, 1200 Å, and 2000 Å). For each thickness the 'Al metal' control data are presented first, followed by the 'Base metal' data and the 'Beam-leaded' data on facing pages. The same format is used for the V_{TN} histograms in Figs. 10 through 18. The histograms are shown here to allow comparison of the distributions for aluminum control wafers with the wafers in the beam-lead processing.

*In these histograms, the ordinate is normalized to the number of readings in the histogram cell with the largest population. The abscissa is divided into 100 cells and the units are in volts. On the right-hand side of each histogram are listed the upper and lower limits of the test, the number of units exceeding each limit, the total number of units tested, and the number in the most populated cell. The arithmetic mean and one sigma value are also listed. The 'mean' values differ slightly from the 'average' values for V_T listed in Table 2.

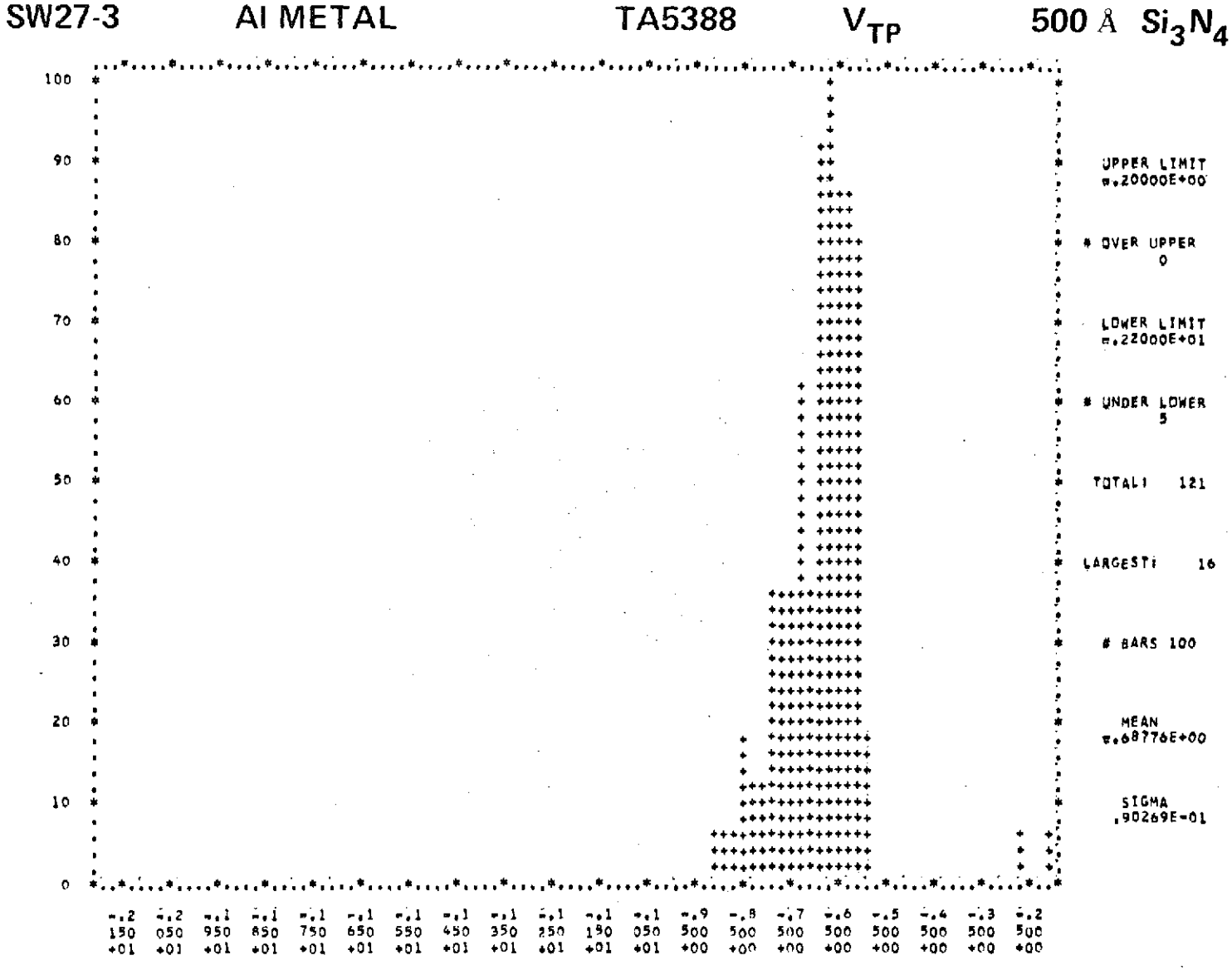

Figure 1. SW27-3, Al metal, TA5388, V_{TP}, 500 Å Si_3N_4.

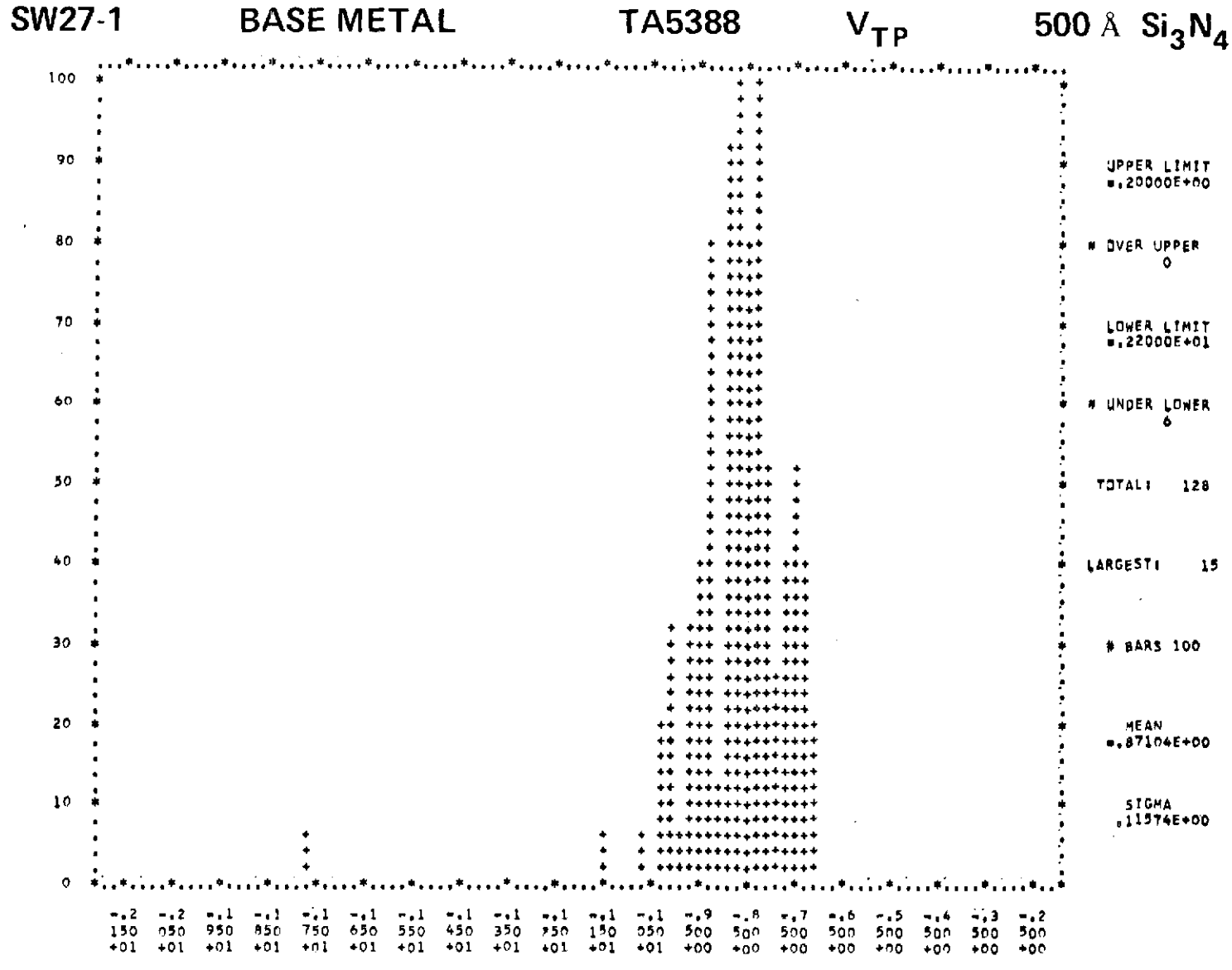

Figure 2. SW27-1, Base metal, TA5388, V_{TP}, 500 Å Si_3N_4.

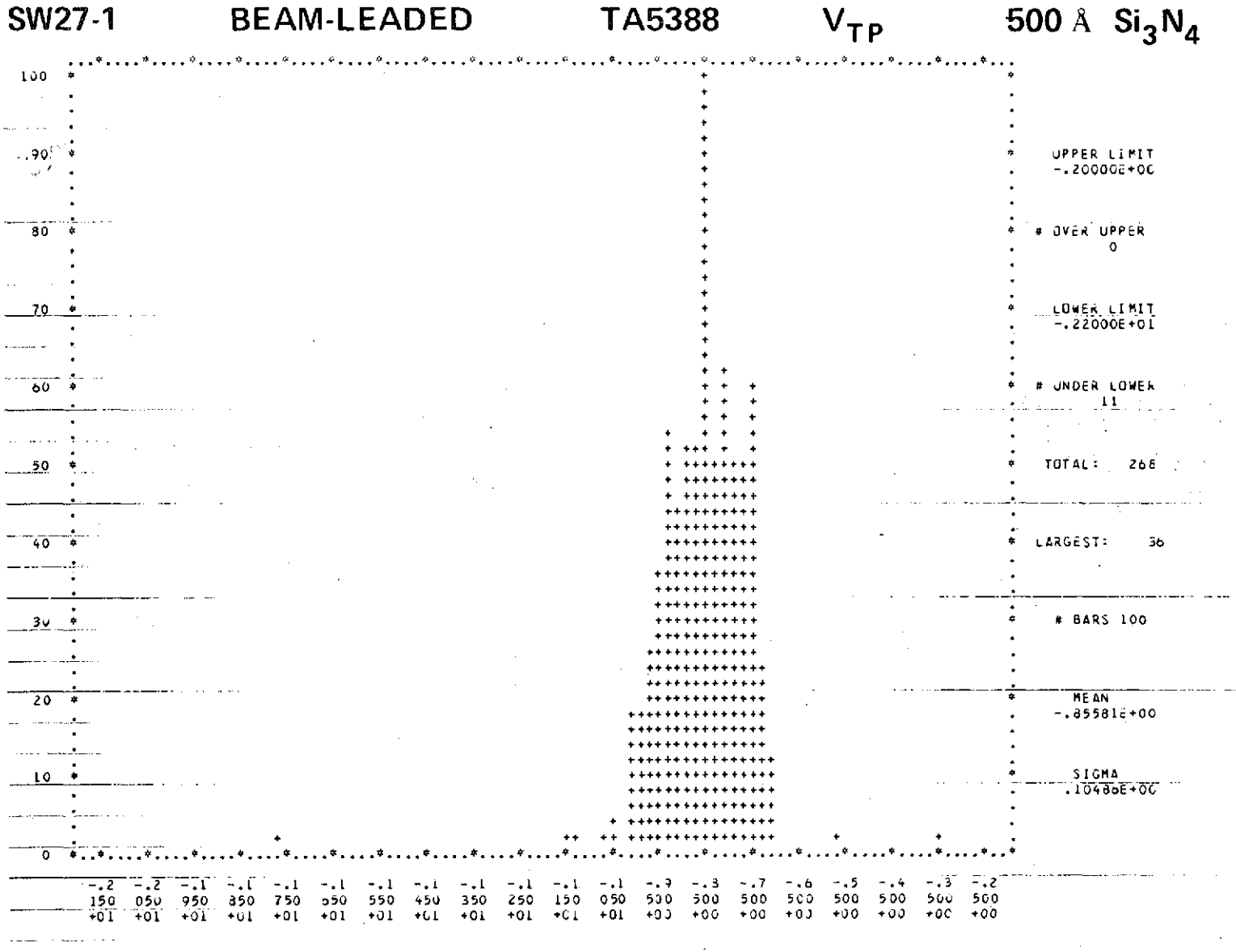

Figure 3. SW27-1, Beam-leaded, TA5388, V_{TP}, 500 Å Si_3N_4.

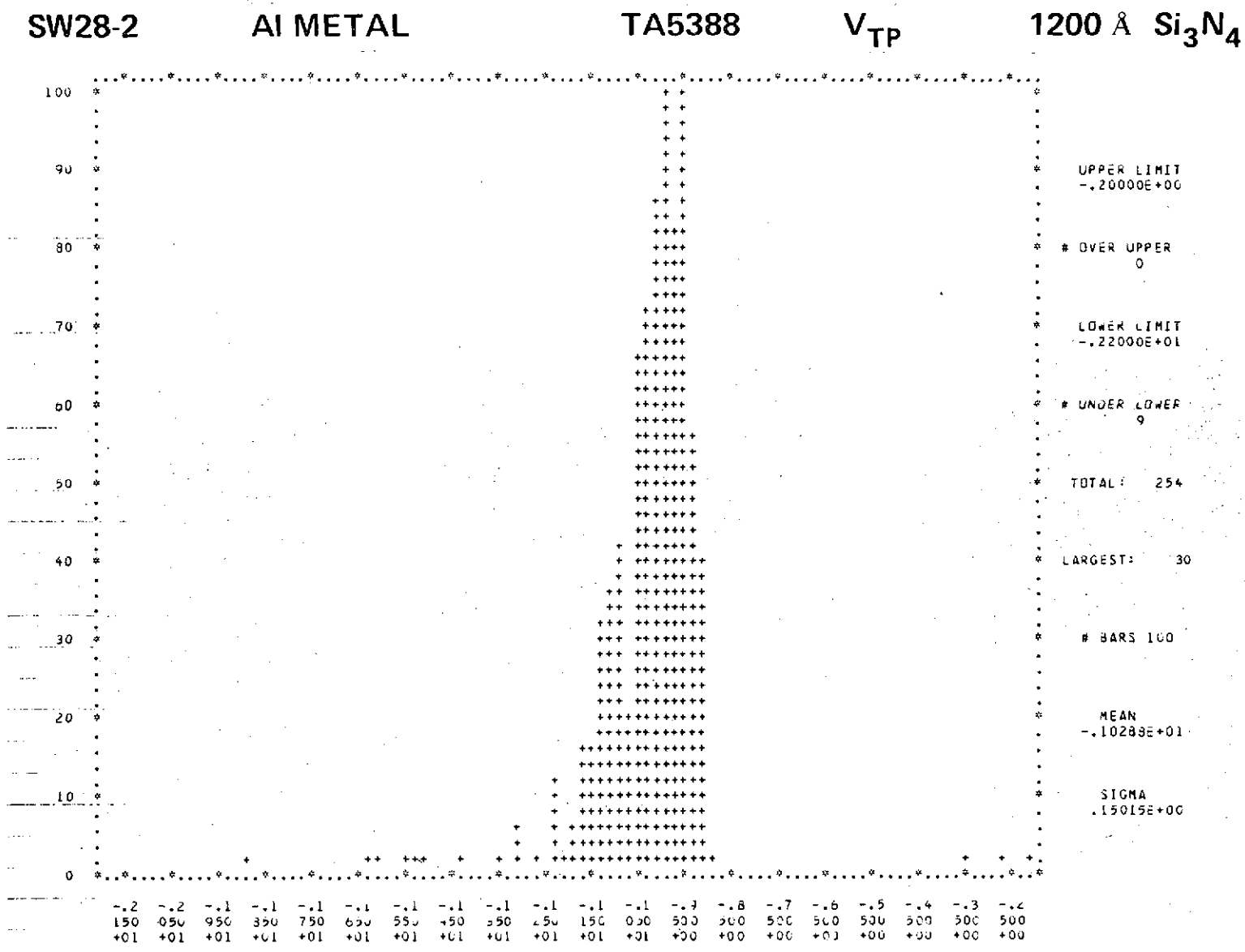

Figure 4. SW28-2, Al metal, TA5388, V_{TP}, 1200 Å Si_3N_4.

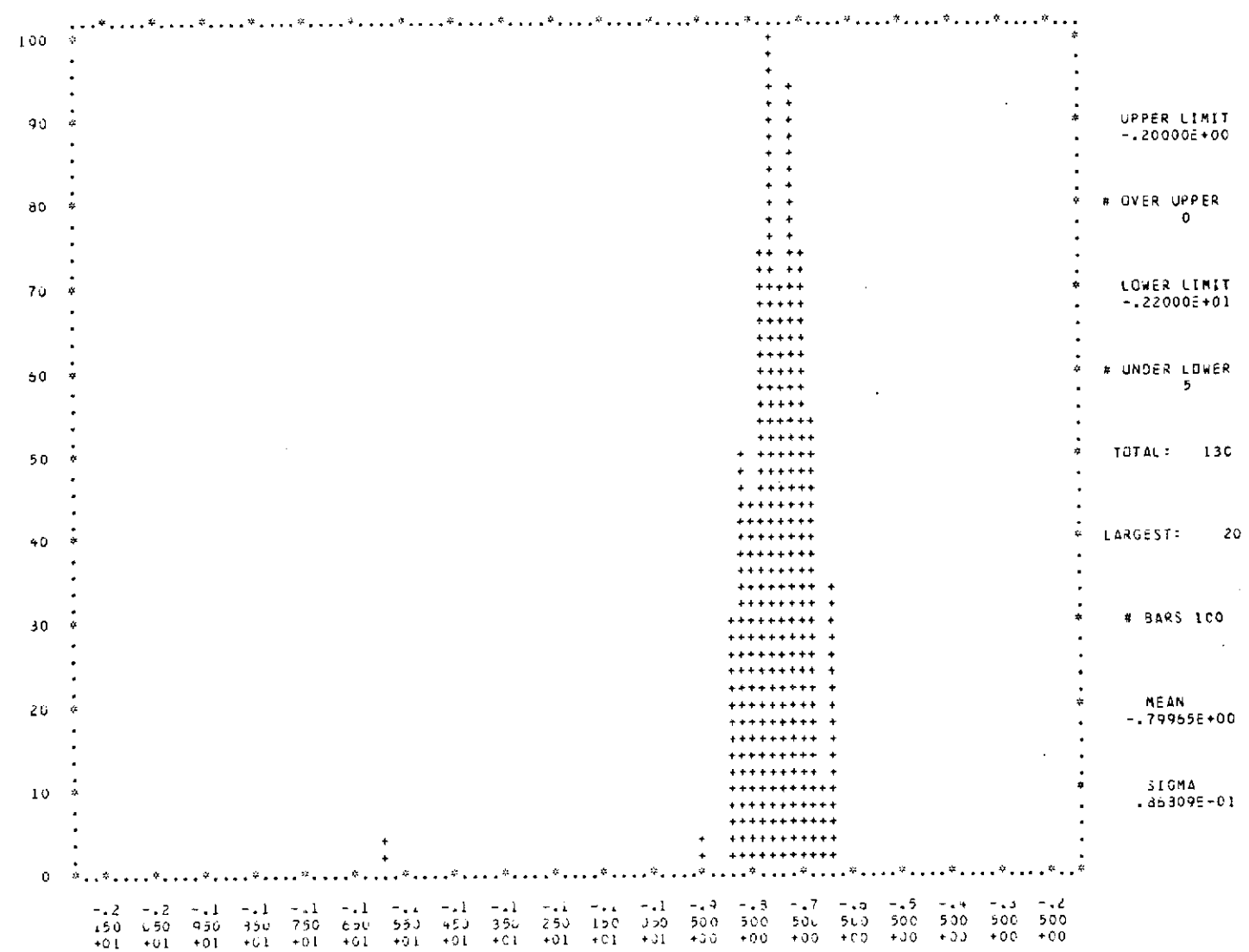

Figure 5. SW28-1, Base metal, TA5388, V_{TP}, 1200 Å Si_3N_4.

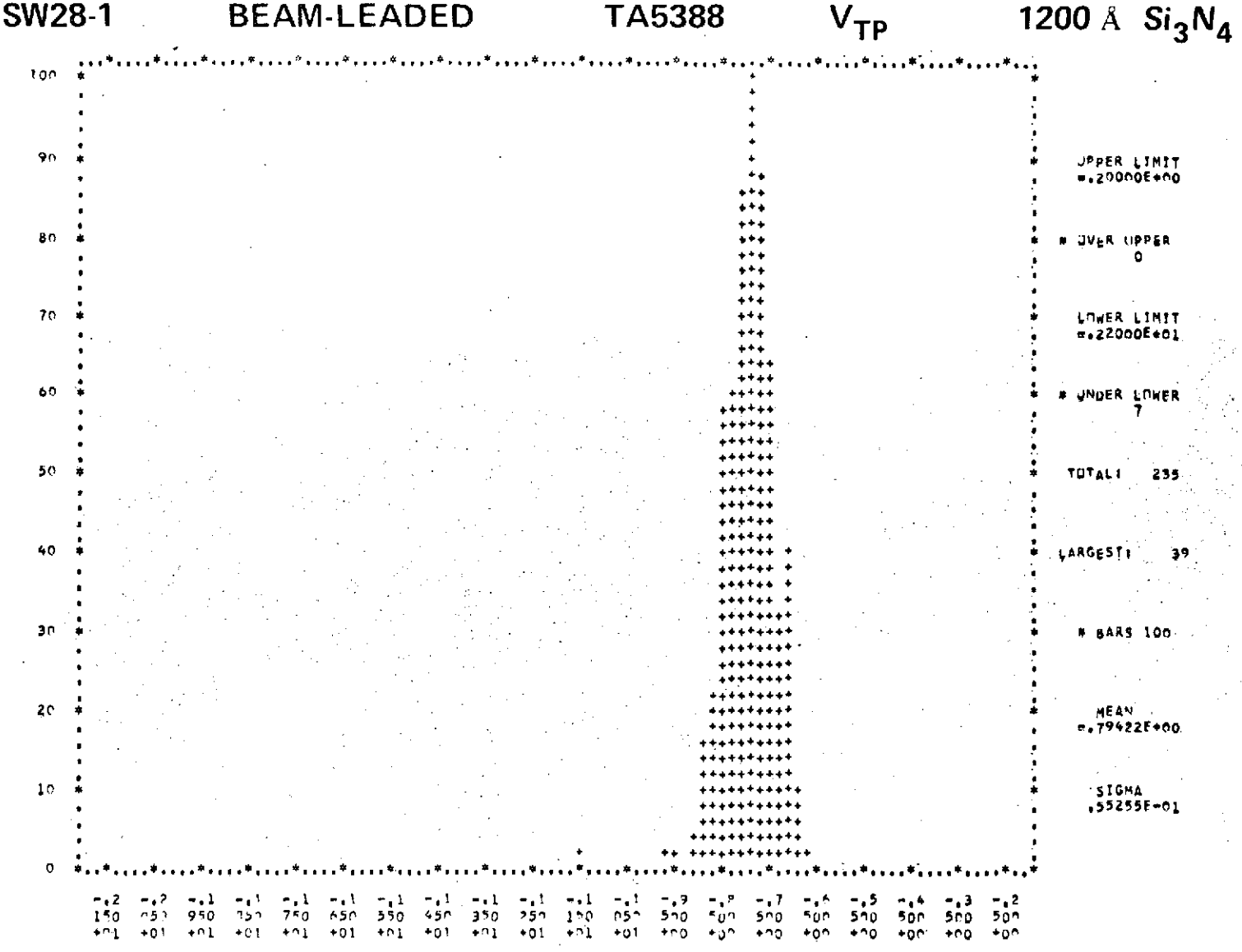

Figure 6. SW28-1, Beam-leaded, TA5388, V_{TP}, 1200 Å Si_3N_4.

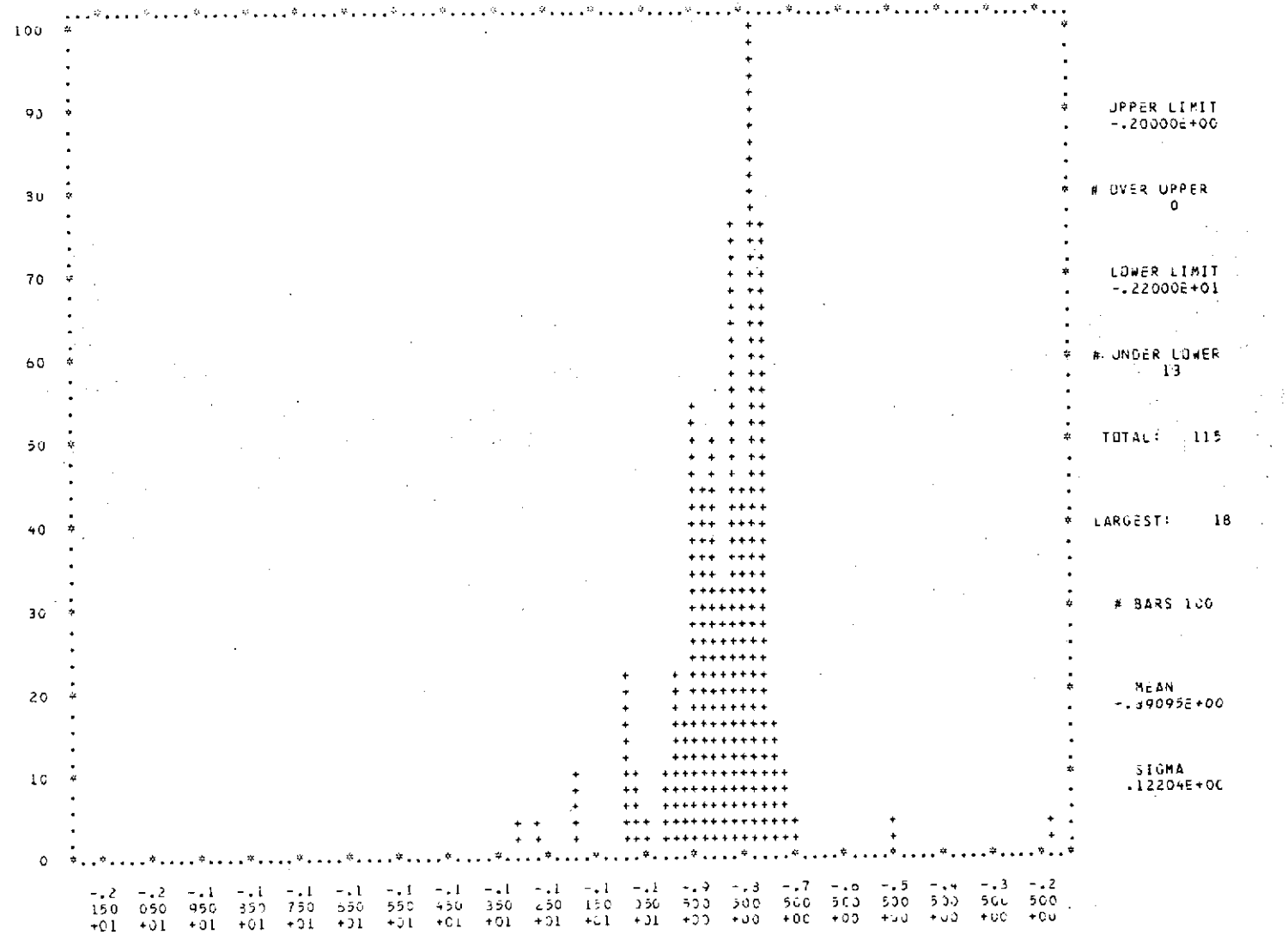

Figure 7. SW28-5, Al metal, TA5388, V_{TP}, 2000 Å Si_3N_4.

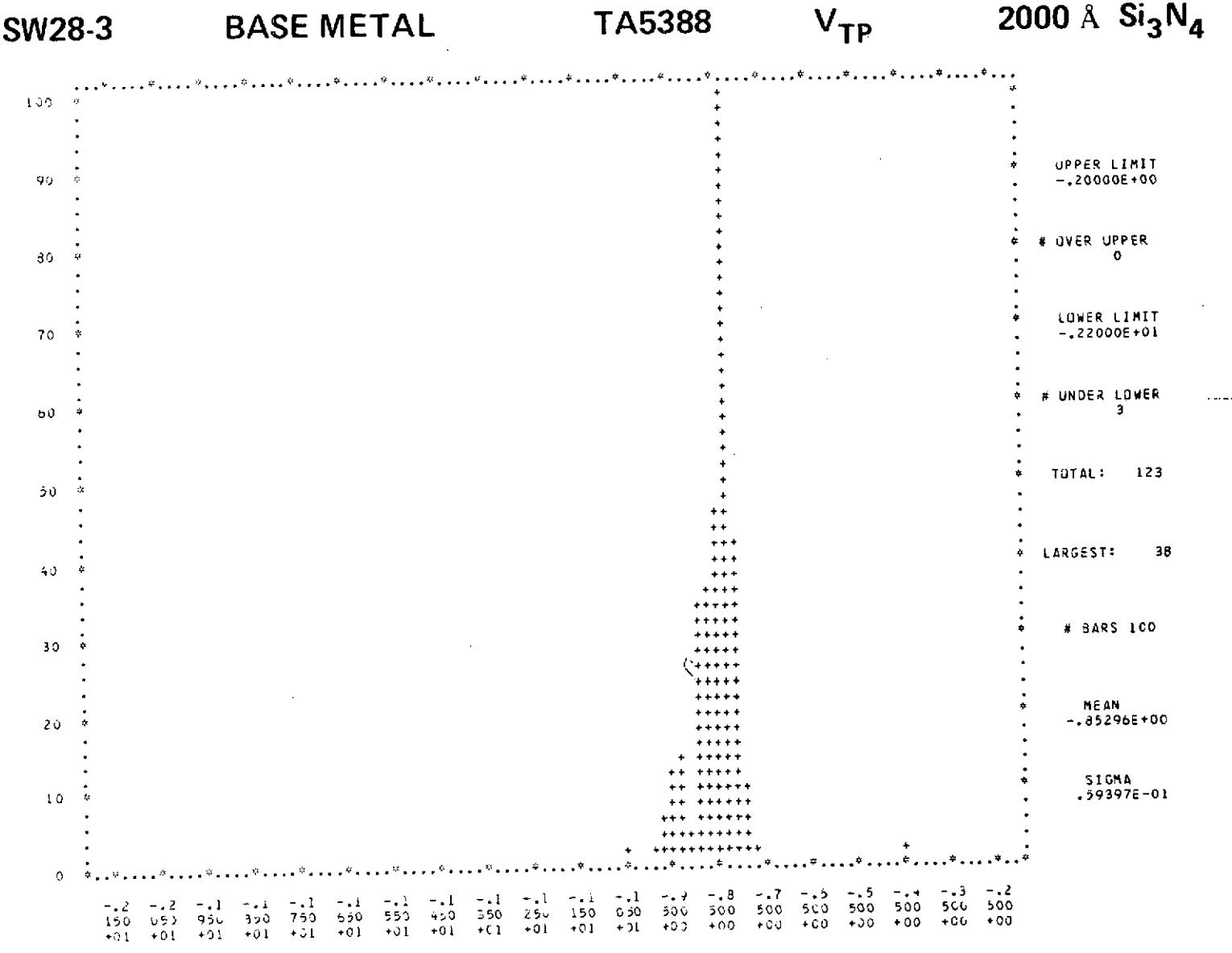

Figure 8. SW28-3, Base metal, TA5388, V_{TP}, 2000 Å Si_3N_4.

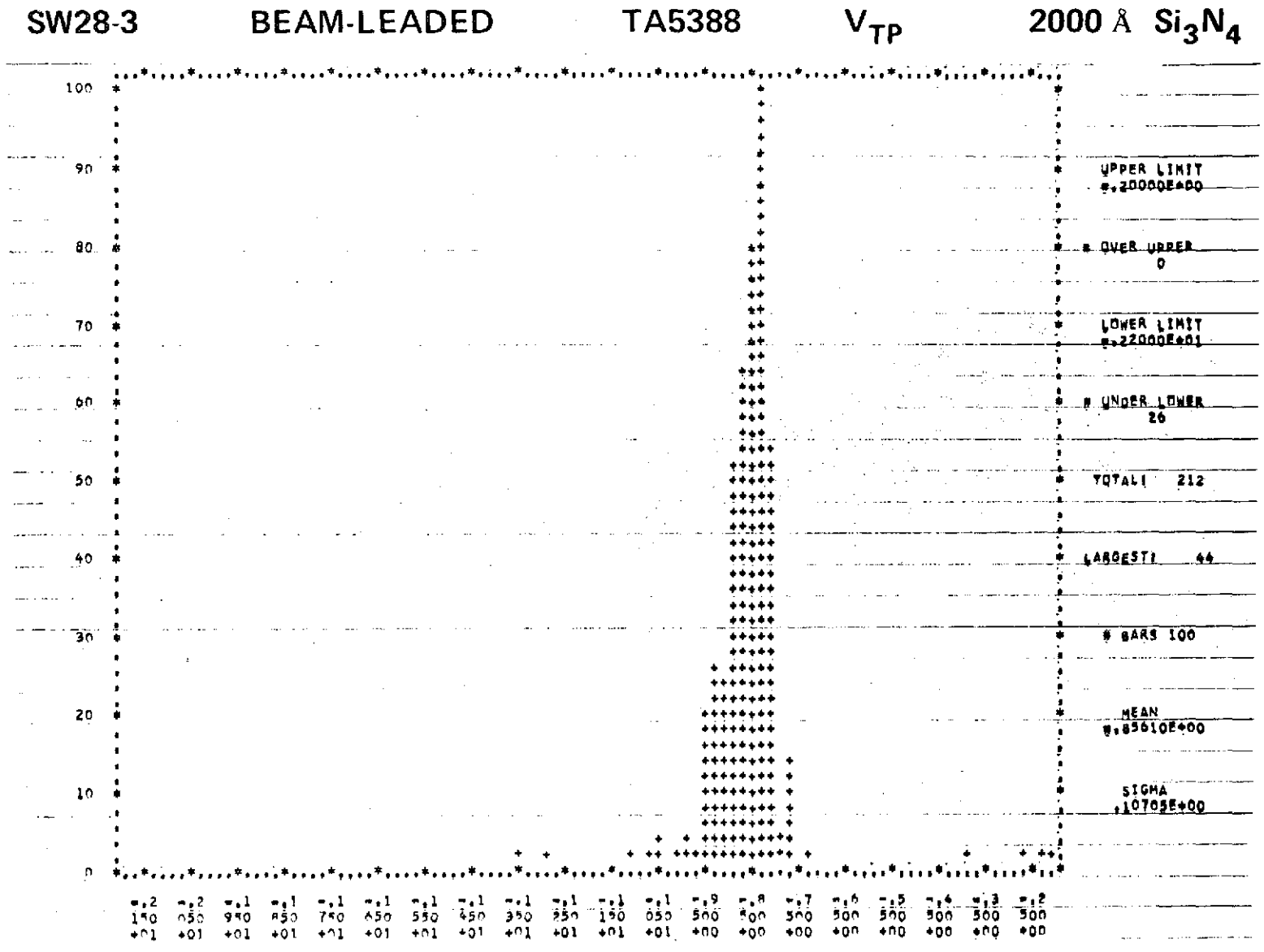

Figure 9. SW28-3, Beam-leaded, TA5388, V_{TP}, 2000 Å Si_3N_4.

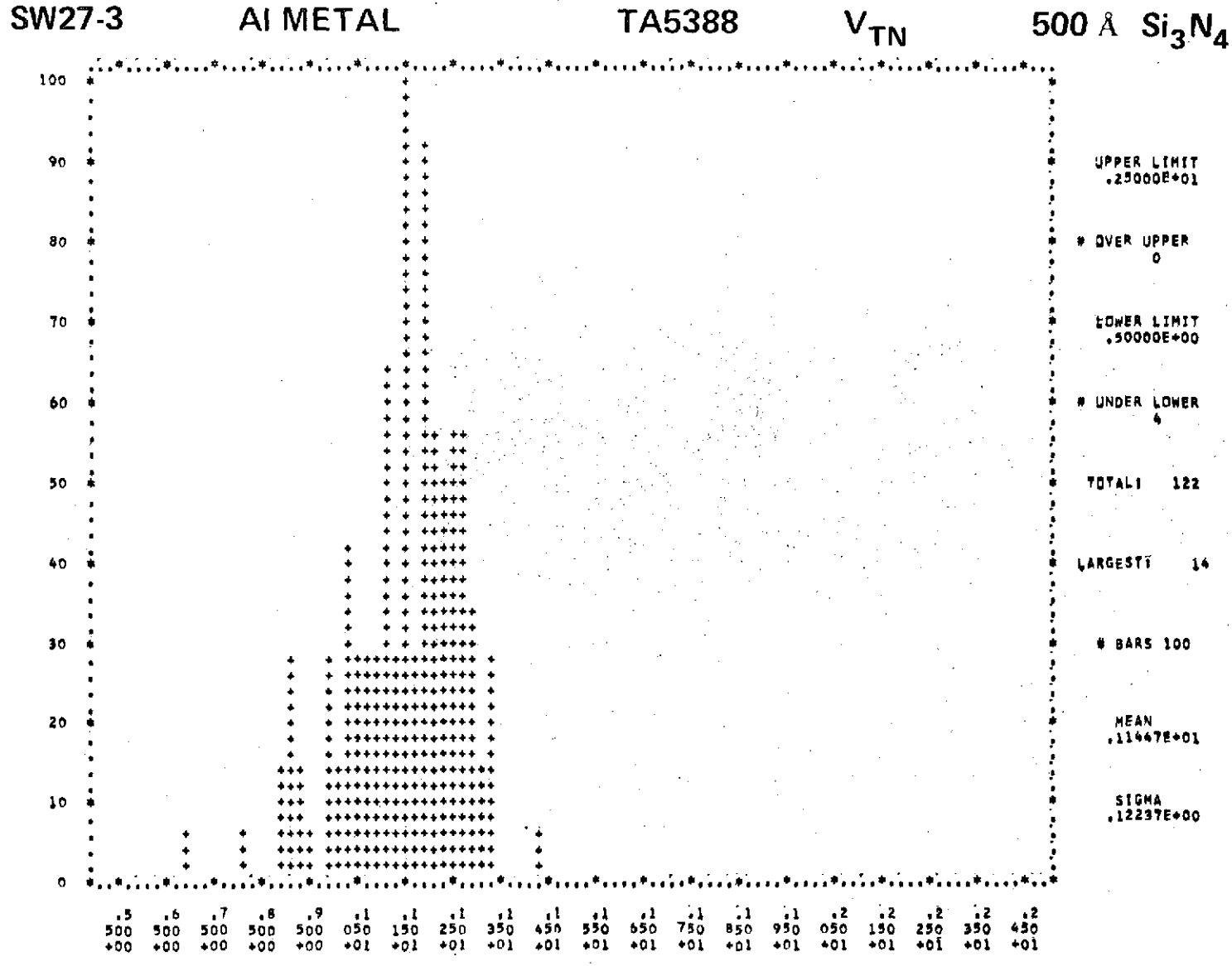

Figure 10. SW27-3, Al metal, TA5388, V_{TN}, 500 Å Si_3N_4.

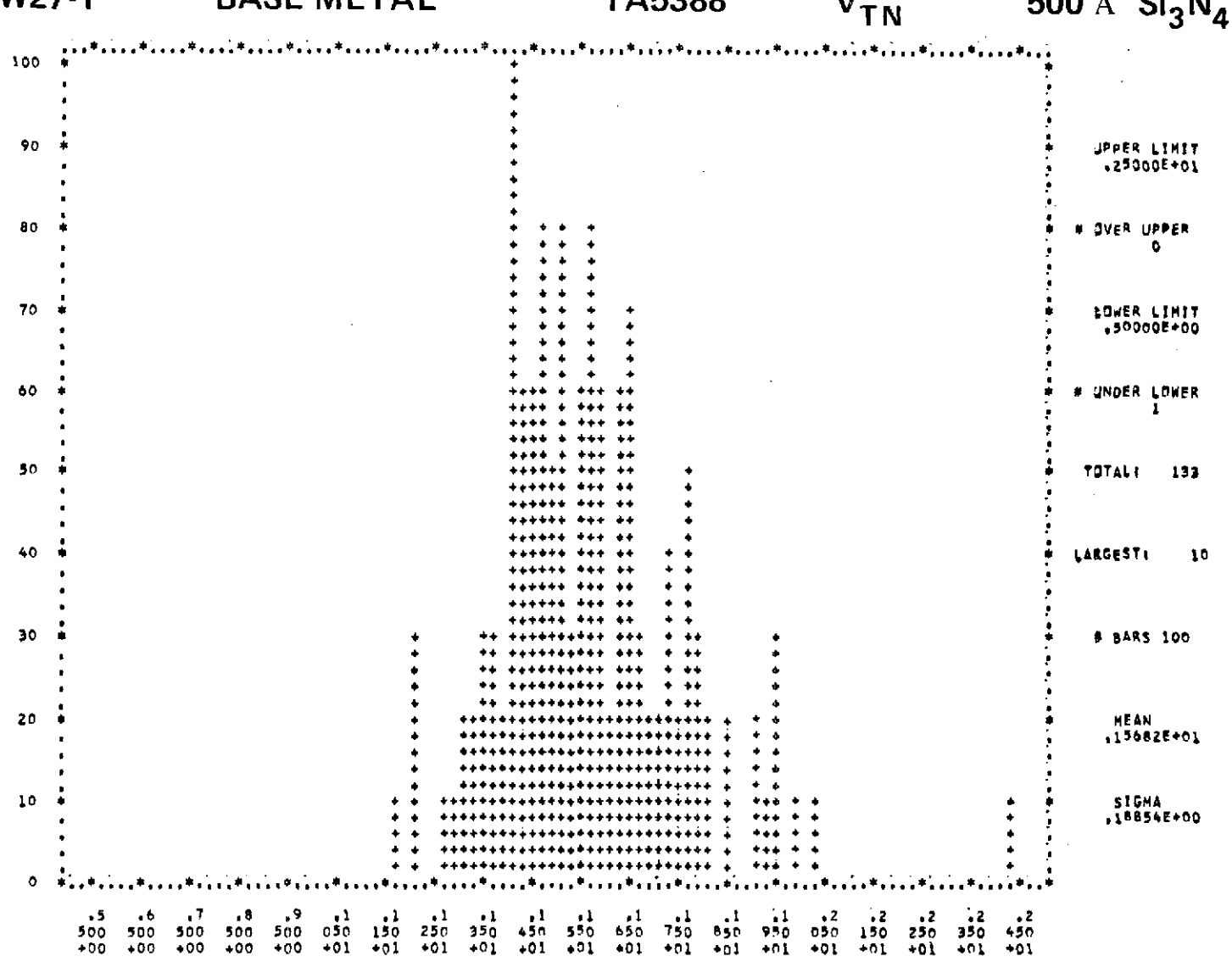

Figure 11. SW27-1, Base metal, TA5388, V_{TN}, 500 Å Si_3N_4.

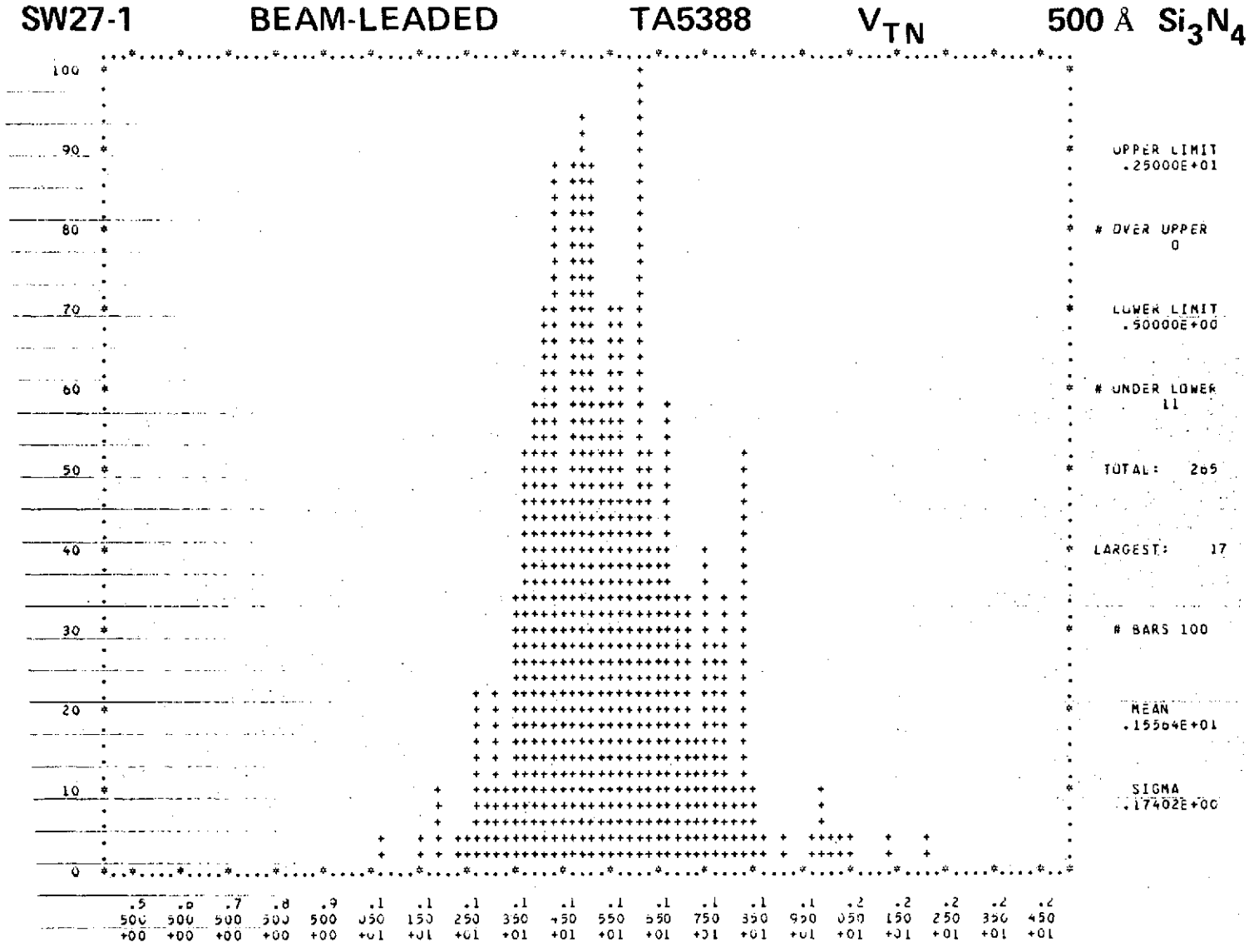

Figure 12. SW27-1, Beam-leaded, TA5388, V_{TN}, 500 Å Si_3N_4.

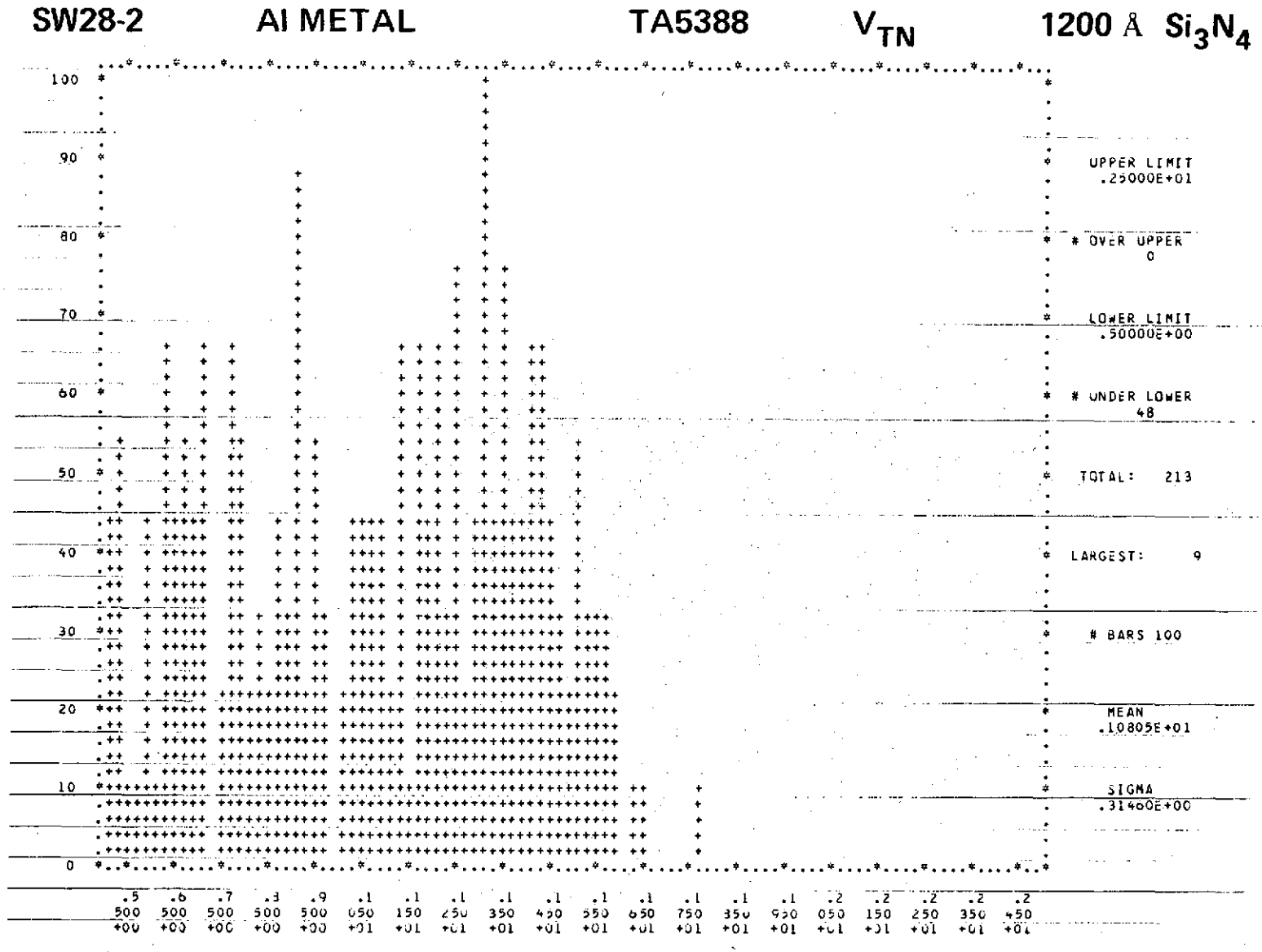

Figure 13. SW28-2, Al metal, TA5388, V_{TN}, 1200 Å Si_3N_4.

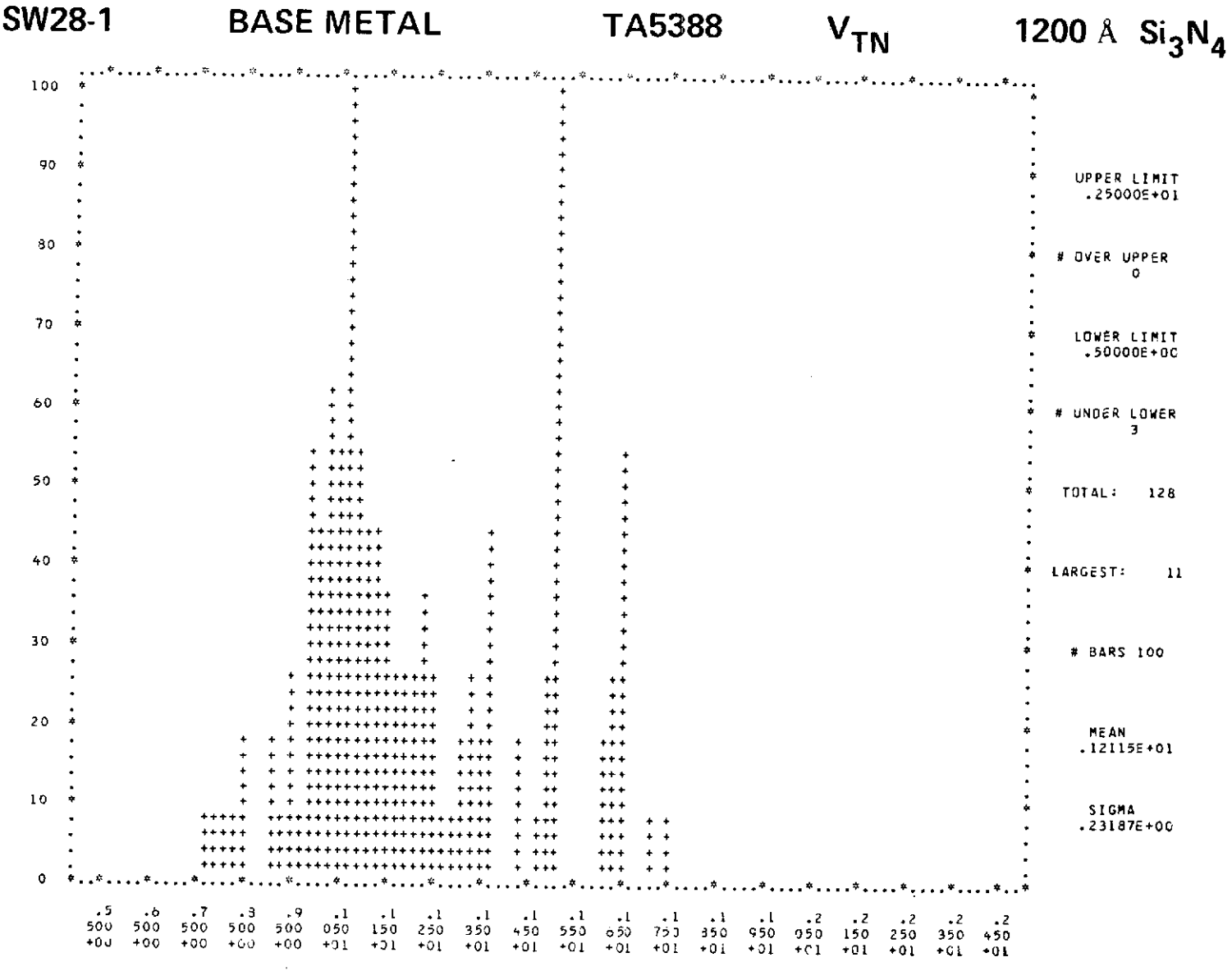

Figure 14. SW28-1, Base metal, TA5388, V_{TN}, 1200 Å Si_3N_4.

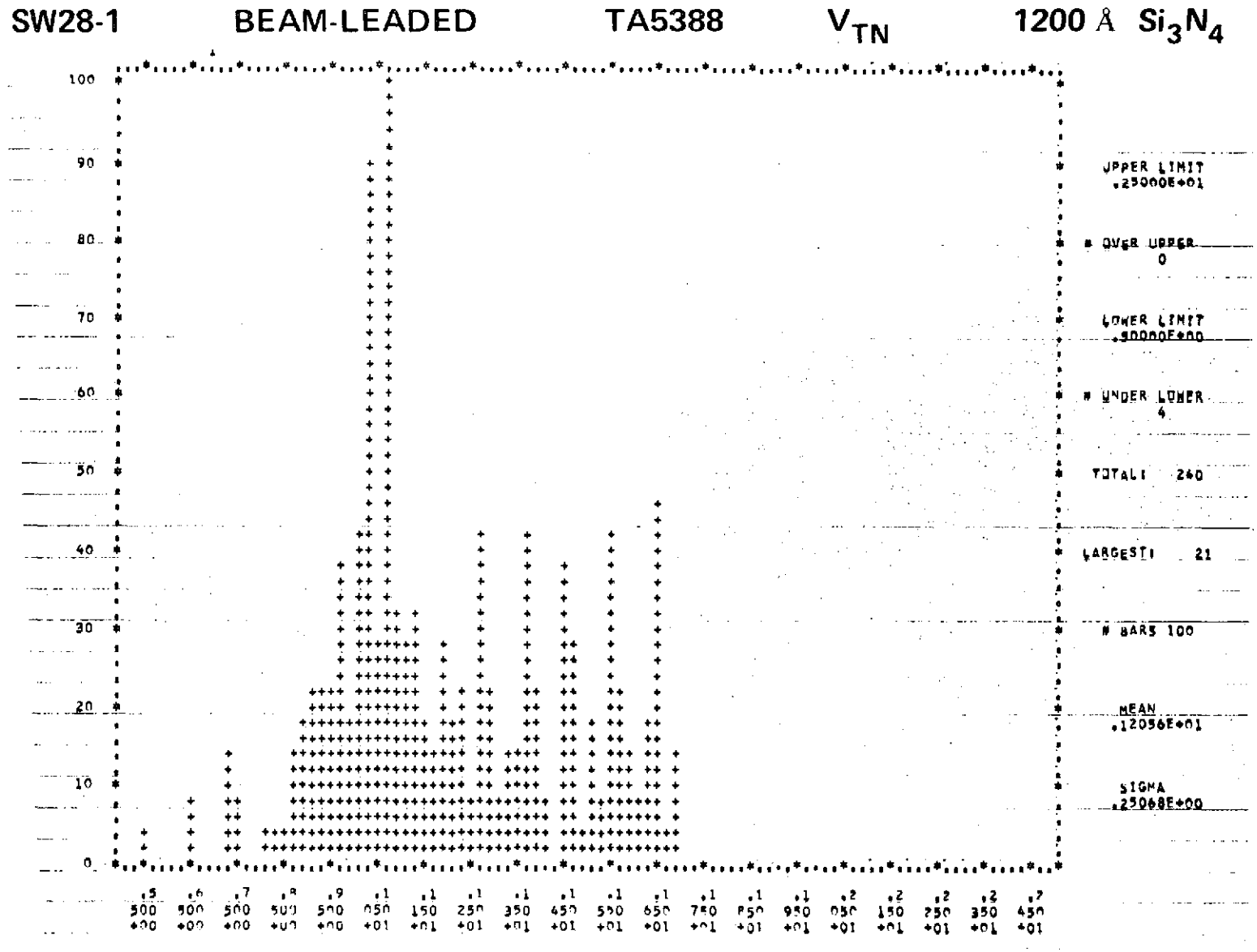

Figure 15. SW28-1, Beam-leaded, TA5388, V_{TN}, 1200 Å Si_3N_4.

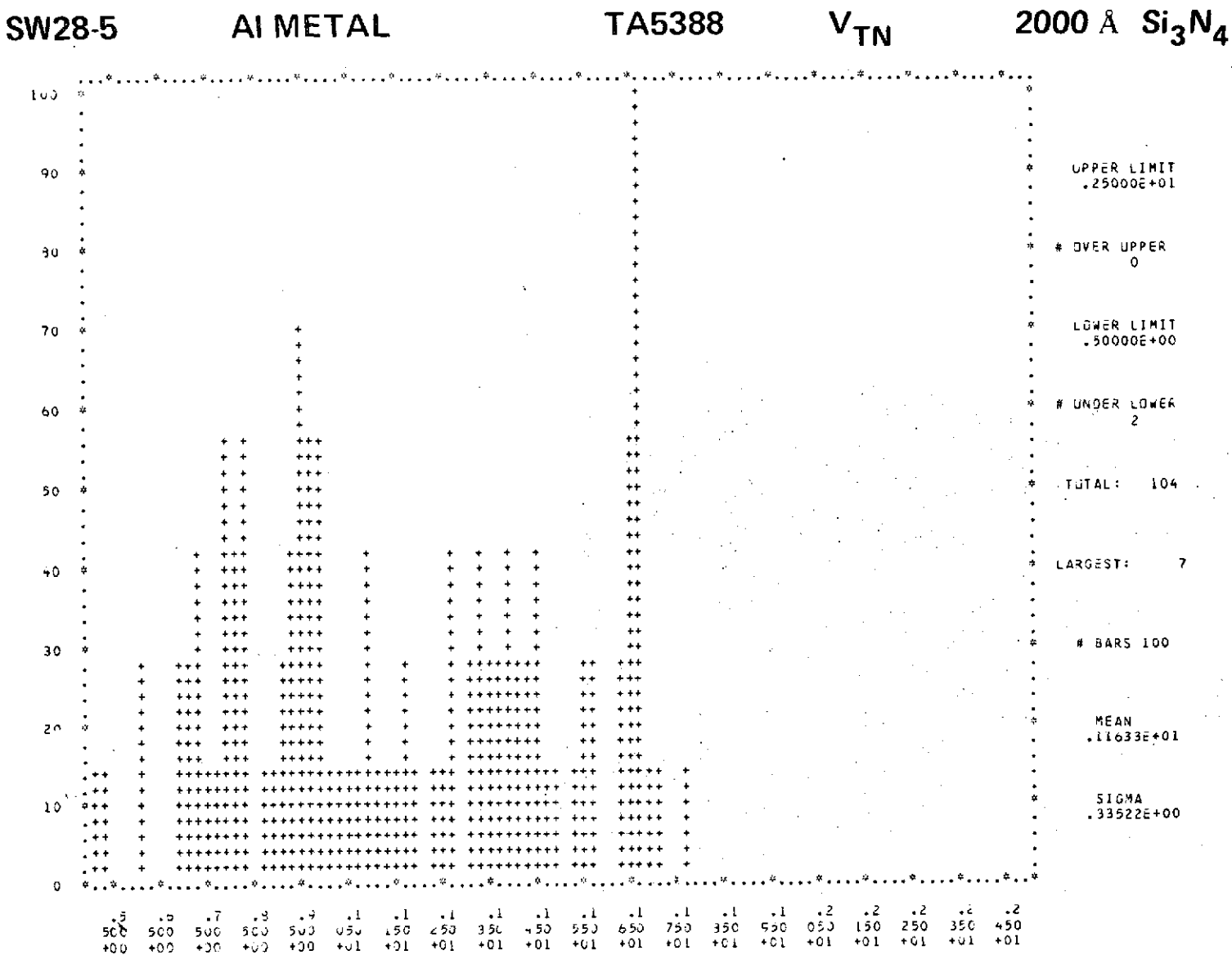

Figure 16. SW28-5, Al metal, TA5388, V_{TN}, 2000 Å Si_3N_4.

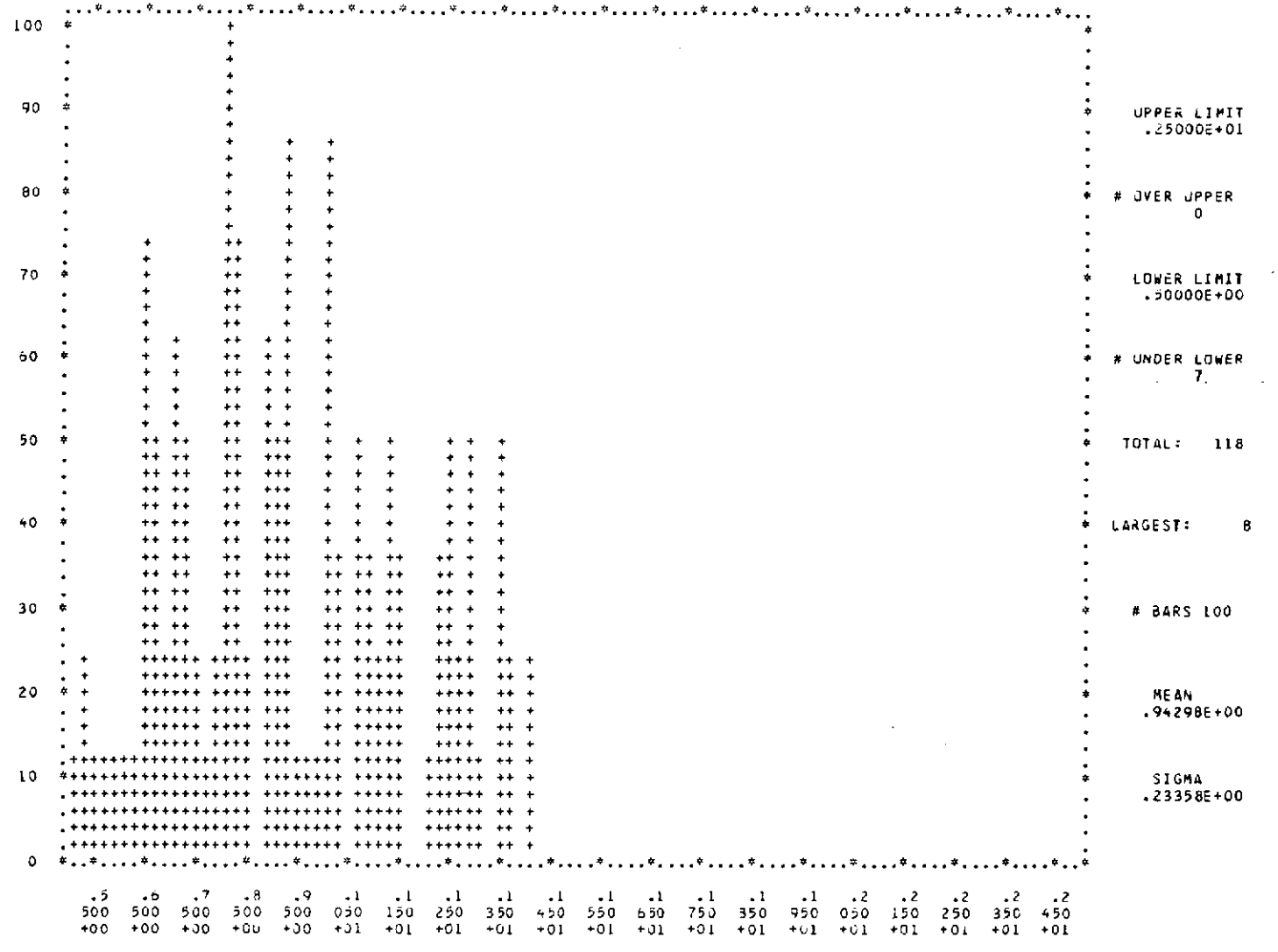

Figure 17. SW28-3, Base metal, TA5388, V_{TN}, 2000 Å Si_3N_4.

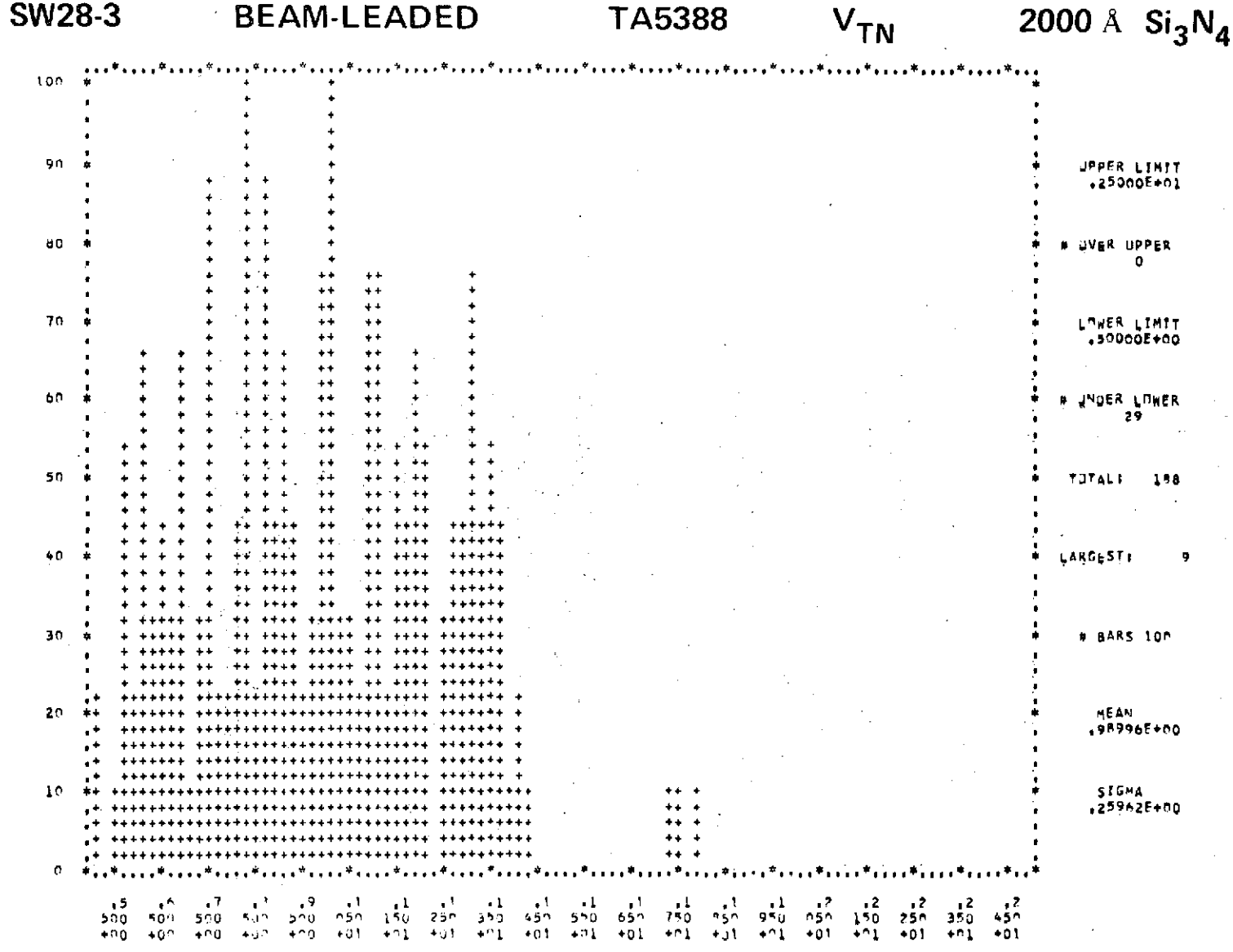

Figure 18. SW28-3, Beam-leaded, TA5388, V_{TN}, 2000 Å Si_3N_4.

III. ELECTRICAL RESULTS ON THE BEAM-LEADED SOS TA6567 256-BIT RAM CIRCUIT

Wafer probe testing of the beam-leaded silicon-gate 256-word by 1-bit static SOS CMOS RAM designated as the TA6567 has demonstrated that there are functionally perfect units after base-metallization and after beam formation processing. Units have been found, using the MD-100 memory exerciser, which successfully pass MARCH, MASEST, GALPAT, and WAKPAT test routines. Beam-leaded packaged units have not been available for further testing. The above results were on the first lot of fully beam-leaded TA6567 wafers, and the overall yield was very low. The present processing efforts are to increase the through-put of TA6567 beam-leaded wafers and to obtain packaged beam-leaded circuits for additional testing. Figure 19 is a photograph of the beam-leaded TA6567 chip on the 24-pin DIP ceramic package.

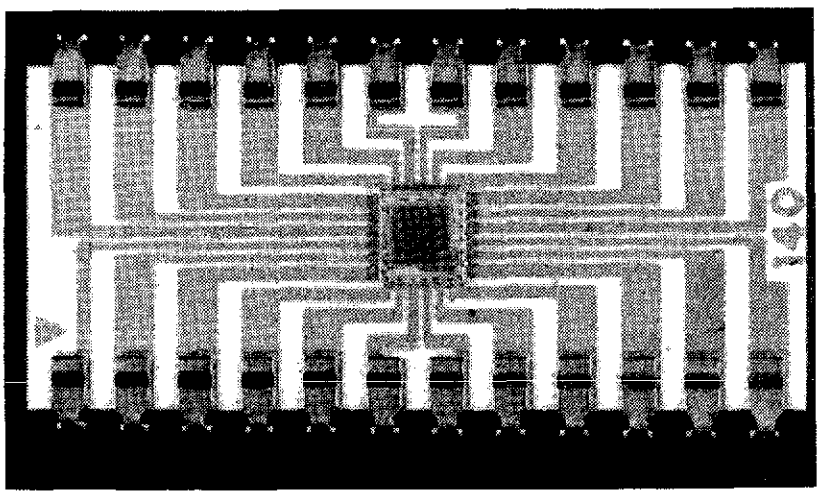

Figure 19. TA6567 BL/SOS 256-bit RAM chip bonded onto a 24-pin DIP ceramic package.

A detailed discussion of the modification and redesign of the beam-leaded RCA TA6473 256-word by 1-bit static SOS/CMOS RAM for the beam-lead technology was given in a previous report [1]. The redesigned version (designated TA6567) also included circuit enhancements to improve the functional performance of the memory. Figure 2 in the above report compared the measured read access time, t_{AC}, as a function of load capacitance upon the outputs (D_{out} and $\overline{D_{out}}$) for the TA6473 circuit with the computer-aided-design simulations for the TA6567 circuit. The plot is reproduced in this report as Fig. 20, and the recently measured data for the TA6567 circuit is included for comparison. The data reported here are for packaged chips with aluminum metallization, and no major change is expected for chips with beam-lead metallization.

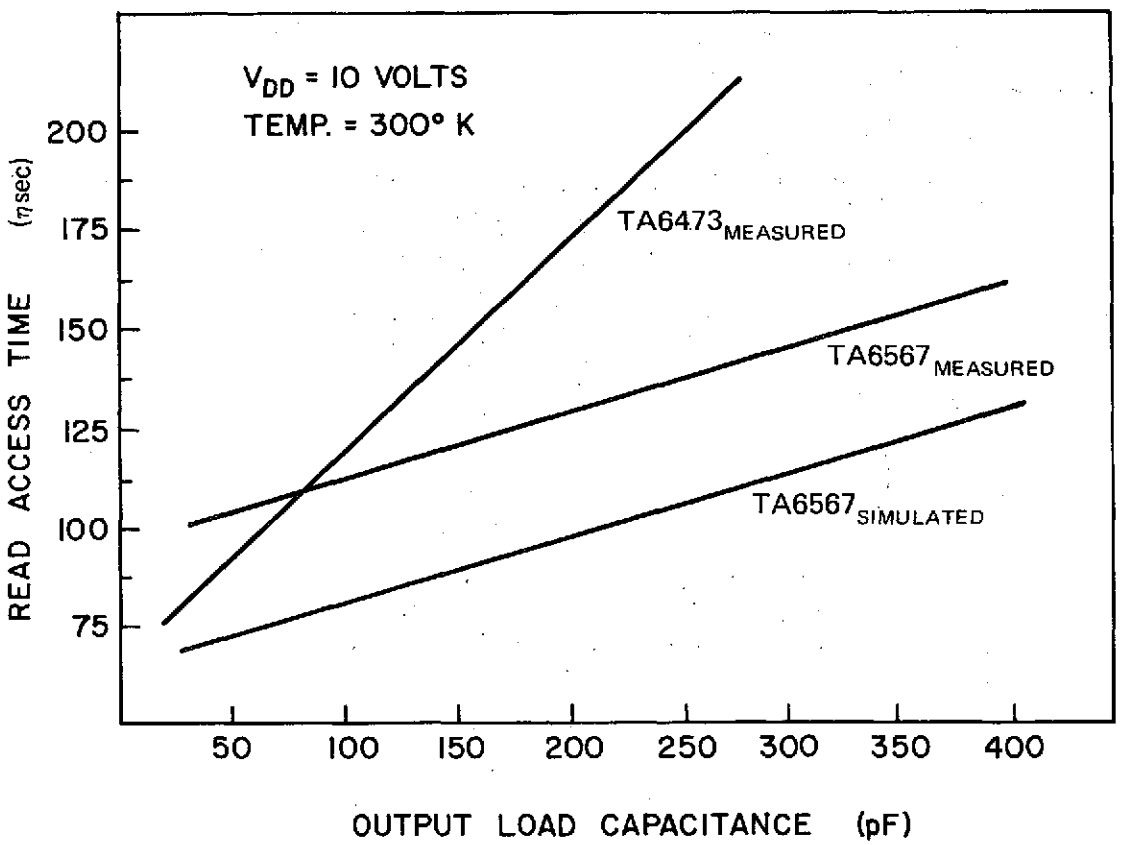

Figure 20. Read access time as a function of output load capacitance for both the TA6473 circuit and the TA6567 circuit.

Enhanced performance at the larger loads for the TA6567 circuit is readily apparent from the illustration for both the measured and simulated data. The constant offset between these two curves occurs because, in the simulation using the R-CAP program, only a first approximation for the capacitance was made. The Δt_{AC} between these two curves is related to the remaining internal RC network affecting the access time. Also note that the response of the TA6567 circuit is slower compared with that of the TA6473 circuit at low values of output capacitance. This is to be expected because the output drivers of the TA6567 were increased in current drive capability to improve t_{AC} for larger relative capacitances. This modification added extra loading to the internal memory circuitry that controls the drivers that, in turn, would degrade the first stage of the read access time process. This was a design trade-off that increased the "fixed" delay of the output turn-on while reducing the rise and fall transition periods and hence improving the total circuit response for larger loads. The performance gained by the enhanced output drive is desirable for a system implementation of RAM's onto a memory plane where larger fan-out is needed.

IV. PERSONNEL AND EXPENDITURES

During the quarter reported herein the following personnel contributed to the contract:

W. C. Schneider	Project Scientist

Total expenditures through September 30, 1974, have been $233,839, including profit. Problem areas that may create an overrun: none at this time.

V. NEW TECHNOLOGY APPENDIX

It was concluded from the review of the work that there were no reportable items of New Technology under the contract during the period covered by this report.

ACKNOWLEDGMENTS

The author wishes to acknowledge the informative discussions with R. J. Hollingsworth and the processing help given by D. Tanguay.

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1. W. C. Schneider, Design, Processing, and Testing of LSI Arrays for Space Station, Quarterly Technical Report No. 14, Contract NAS12-2207, August 1974.